VLSI Implementation of a Simple Spiking Neuron Model

Abdullah H. Ozcan
Vamshi Chatla
ECE 6332 – Fall 2009
University of Virginia
aho3h@virginia.edu
vkc5em@virginia.edu

ABSTRACT

In this paper, we design a threshold inverter quantization (TIQ) based analog to digital converter (ADC) for a CMOS neuron circuit. We also study a neuron circuit and use inverter as a comparator in that design to reduce power consumption.

1. INTRODUCTION

The complexity of human brain is amazing when it is compared to today's cutting edge computers. It has approximately 100 billion neurons. Understanding this huge neuron network's working behavior has always been an important task for researchers. To accomplish that it is important to understand single neuron's behavior.

Due to the increasing interest in neural networks, there are many VLSI neuron models proposed in the literature. However, most of them suffer from different properties like threshold variability, simplicity, allowing different types of neurons, etc. Among these neuron models the most common used one is integrate and fire neuron model. Izhikevich proposes a simple model for simple spiking neurons [1].

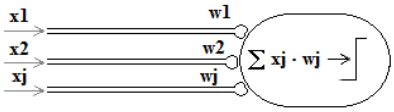

Figure 1. Single neuron and synapses

In a human brain each neuron has synapses of between 10-10^5. The input currents going to a single neuron is integrated in it's dendrite and then neuron fires if the integrated inputs exceeds neuron's threshold. The strength of those inputs depends on the weight of each synapse. Because of that high number of neurons and synapses it is important to design a low power neuron circuit.

In this paper we design a TIQ based ADC circuit to be used for converting analog weights into digital form. After that we explain CMOS circuitry that implements the Izhikevich's neuron model and use inverter as a comparator in that design to reduce power consumption.

2. TIQ BASED ADC CIRCUIT

Here we designed a 4 bit TIQ based ADC circuit. Since threshold inverter quantization (TIQ) technique is started to used in ADC designs[4], its growing interest continues because of its significant speed, reduced area and low power consumption.

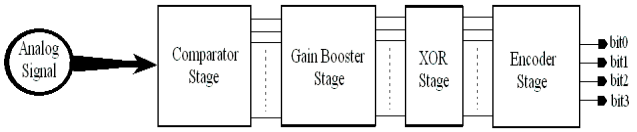

Figure 2. TIQ Based ADC circuit block diagram

The idea is to use inverter as a voltage comparator. The simplicity in the design of the comparator part provides both high speed and low power consumption at the same time. Figure 1 shows the block diagram of the TIQ flash ADC.

Different comparator threshold voltages are determined by systematic transistor sizing. The threshold voltage of the comparator can approximately given in the following equation.

$$Vth = \frac{Vdd - |Vtp| + Vtn\sqrt{Kn/Kp}}{1 + \sqrt{Kn/Kp}} \quad (1)$$

$$Kn = (W/L)_n \cdot \mu n \, Cox$$
$$Kp = (W/L)_p \cdot \mu p \, Cox \quad (2)$$

Vtn and Vtp are the threshold voltages of the NMOS and PMOS transistors in the inverter. Although the equation given above is giving us an idea how the threshold voltage of the comparator changes for different supply voltage, Wn and Wp, because of the non-idealities of the transistors, that equation cannot be used to determine the exact threshold voltages.

In the comparator block there are two cascaded and systematically sized inverters used. For a 4 bit ADC design, sixteen equally spaced threshold voltages in the desired analog range is needed. After some amount of simulations we determined these threshold voltages. Figure 2 shows the output of comparator block.

The gain booster stage consists of two cascaded identical inverters unlike the comparator stage. This stage is needed for a full voltage swing and sharper transitions. Otherwise there would be some annoying effects like unbalanced delays and different voltage swings at the output of ADC.

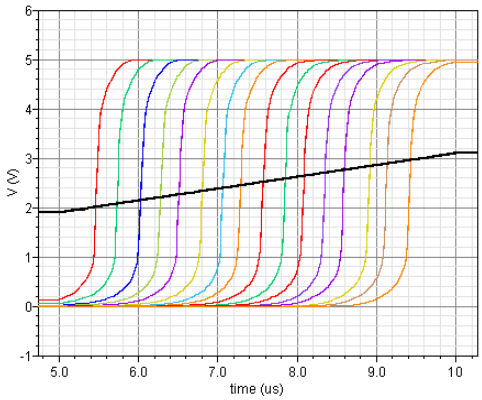

Figure 3. Threshold Levels of 4 bit ADC circuit

The output of gain booster stage is called thermometer code (TC). XOR Stage converts this TC code to one-out-of-N code. This stage consists only bunch of xor gates.

Encoder stage converts one-out-of-N code to binary code (BC). Here we used a fat tree encoder. Because of its tree structure, it is faster compared to other types of encoders. A fat tree encoder circuit signal delay is $O(\log_2 N)$, ROM type encoders signal delay is O(N) and wallace tree encoders signal delay is $O(\log_{1.5} N)$ [5].

2.1 ADC Simulation Results

The circuit has been simulated in SPICE using standard 0.6um CMOS technology parameters. Figure 3 shows the output of our ADC circuit. The first slanted line is the analog signal changing in a range of 2-3 volts. The curved lines are the outputs from the comparator due to the analog input signal.

Here we looked at the effects of using different supply voltages for the comparator stage. In Figure 5, comparator threshold voltages as a function of PMOS and NMOS width for different supply voltages is shown. As the supply voltage is increased , the change in the comparator threshold voltage is increased.

For lower supply voltage one would see small changes in comparator threshold voltage. So in order to get same threshold voltage using lower supply voltage, it is needed to increase PMOS width. For instance, if you want to have a threshold voltage of 1.55V using 4.1V Vdd supply, you need to use 1.5 um PMOS width and 2.25 um NMOS width. However if you want to get the same threshold voltage using 3.3V Vdd supply, you need to increase the PMOS width to 3.75 um. You can see these effects in Figure 6.

Reducing power consumption is important for neural network circuits because of the high number of neurons and synapses. Since each synapse would have one ADC circuit to convert analog weight into digital form, even a small power reduction will play an important role. Lowering supply voltage is a way of reducing power consumption.

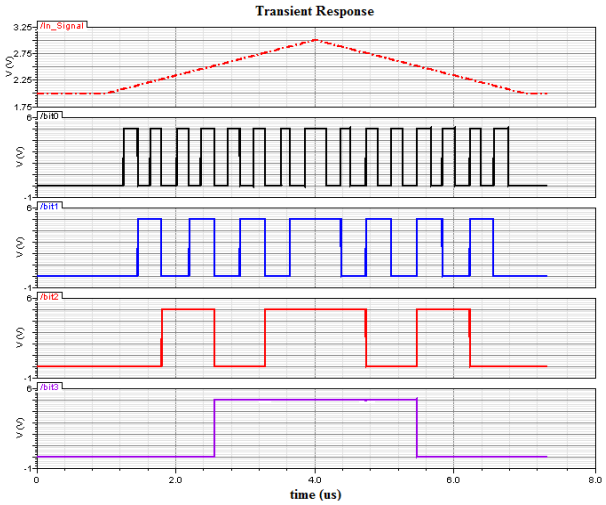

Figure 4. 4 bit ADC

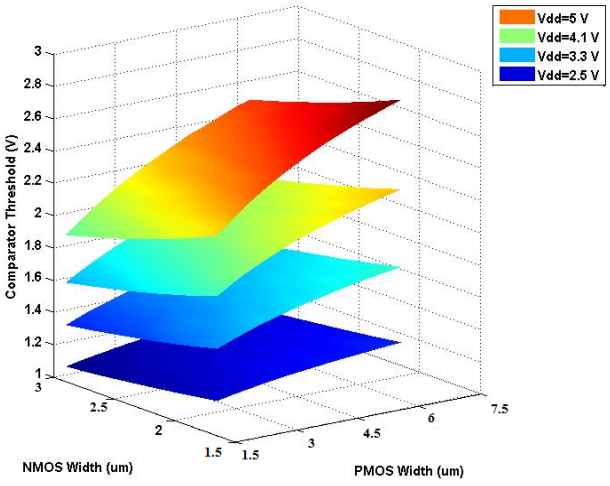

Figure 5. Comparator threshold voltages as a function of NMOS and PMOS width

In the comparator stage, supply voltage affects the threshold voltages of each sixteen equally spaced threshold voltages. So changing supply voltage of comparator stage would change the threshold levels. Keeping Vdd at 5V in the comparator stage and lowering Vdd for the other blocks in ADC gives us some power reduction. Lowering Vdd from 5V to 2.5V, one would get up to 200 uW power reduction.

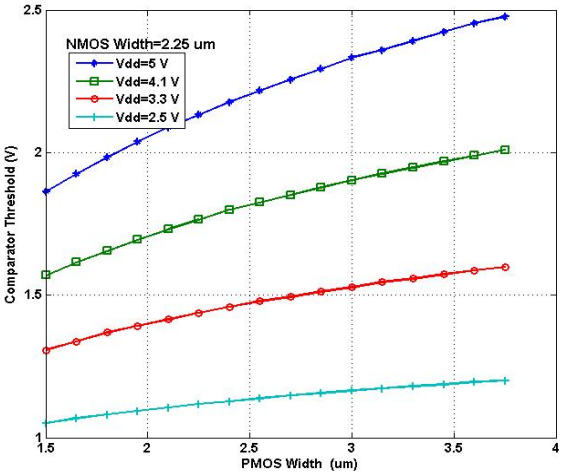

Figure 6. Comparator Threshold Voltages for different supply voltages and PMOS widths (NMOS Width=2.25 um)

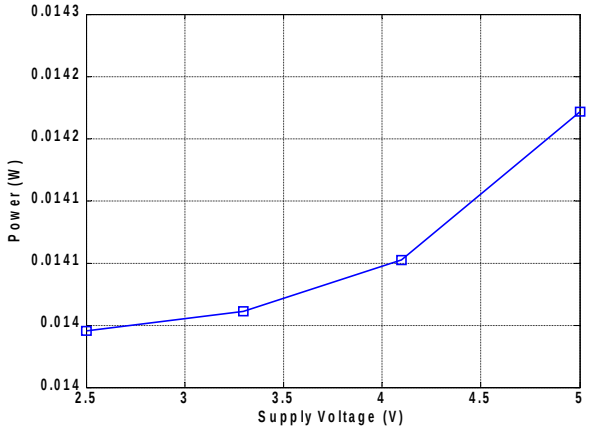

Figure 7. Reducing power consumption by lowering Vdd

Table 1. Power Consumption(Vdd=5V)

ADC	Power (mW)
Comparator	13.37
Gain booster	0.051
XOR('01' Generator)	0.104
Fat Tree Encoder	0.668
Total	14.2

Table 2. ADC Summary

Tecnology	0.6 um
Power	Avg → 14.2 mW Max → 23.9 mW
Transistors	360
Supply Voltage	5V
Analog Range	2-3V
Speed	200 MHz

In the comparator stage, the sized inverters have greater PMOS and NMOS widths compared to other stages of ADC circuit. So comparator stage is the dominant part for power consumption. Aproximately % 94 of the power is consumed by the comparator stage. Because of that small power reduction is achieved by lowering supply voltage.

Impact of variations for the ADC might cause up to circuit failure. For instance, if temperature changes then the mobility, channel length and the threshold voltage of devices will be affected. Simulation results show that if Wp/Wn ratio gets larger, then it is more sensitive to temperature variation. Compared to differential comparator, CMOS inverter is more sensitive to supply voltage noise because of its single-ended input. If Wp/Wn ratio gets larger , then the threshold voltage is more sensitive to supply voltage variations [6].

3. NEURON CIRCUIT

Hodgkin-Huxley is a three-dimensional neuron model that describes the behavior of a neuron using differential equations. It is possible to reduce Hodgkin-Huxley neuron model to a two-dimensional system. Izhikevich proposes a simple two-dimensional model for simple spiking neurons.

$$v' = 0.04v^2 + 5v + 140 - u + I \tag{3}$$

$$u' = a(bv - u) \tag{4}$$

$$\text{if } v \geq Vth \quad v = c;\ u = u + d \tag{5}$$

In the equation above 'v' represents the membrane voltage of the neuron and 'u' is slow state variable which is the inhibition factor for the neuron and controls the firing rate. If the membrane voltage of the neuron exceeds a threshold value then it fires and 'v' is reseted to 'c', and also 'u' is reseted to 'u+d'. Firing rate of the neuron can be increased by lowering the threshold voltage of or by increasing 'a' or by decreasing 'd'. Using this model 20 spiking neuron types can be represented. Currently this model looks like the simplest but also the most efficient neuron model proposed so far.

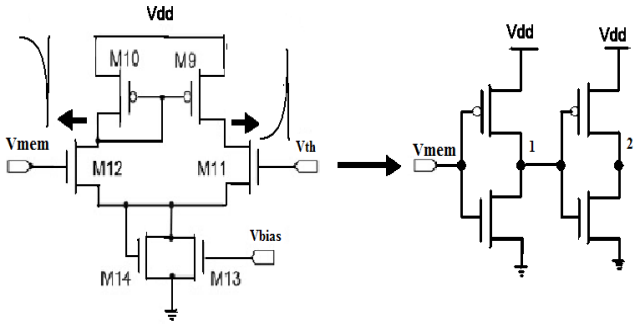

Figure 8. Comparator circuits

Table 3. Proposed neuron circuits[3]

Neuron Model	# Transistors used for 1 Neuron
Conductance-based	27–30+
Integrate-and-fire	18–20
FitzHugh–Nagumo	21
Morris–Lecar	22
Resonate-and-Fire	20
Hindmarsh–Rose	90
Izhikevich	14

B. Wijekoon has been propsed a VLSI neuron circuit using 0.35um CMOS[2]. That circuit takes advantage of nonlinear characteristics of transistors to get the mathematical equations above. The circuit has three parts; membrane potential, slow state variable and comparator. Two capacitors are used for 'v' and 'u' to get each differential equations. The sizes of the transistors are set to meet the desired constants in the equation. So that membrane potential 'v' is achieved by the integration of the currents going to first capacitor and 'u' is achieved by integrating the currents going to the second capacitor.

The third part of the proposed circuit is comparator which detects the spike when the membrane voltage exceeds a specified threshold voltage. This comparator also generates a spike to reset membrane voltage to 'c' and it also generates an inverted spike to pull up the 'u' voltage to 'u+d'. We wrote down current equations for the two capacitors and changed transistors sizes so that the circuit is also working in 0.6um CMOS.

Here we change comparator part of the neuron circuit with an inverter as a comparator. As you can see from Figure 8, when the membrane voltage exceeds the threshold voltage of the comparator, we see a spike in node 2 and an inverted spike in node 1. These spikes in node 1 and 2 are used to reset 'u' and 'v' respectively.

For a 10 us time interval the previous neuron circuit consumes 142.1 mW and the one with new comparator circuit consumes 119.29 mW power. We see % 17 of power reduction.

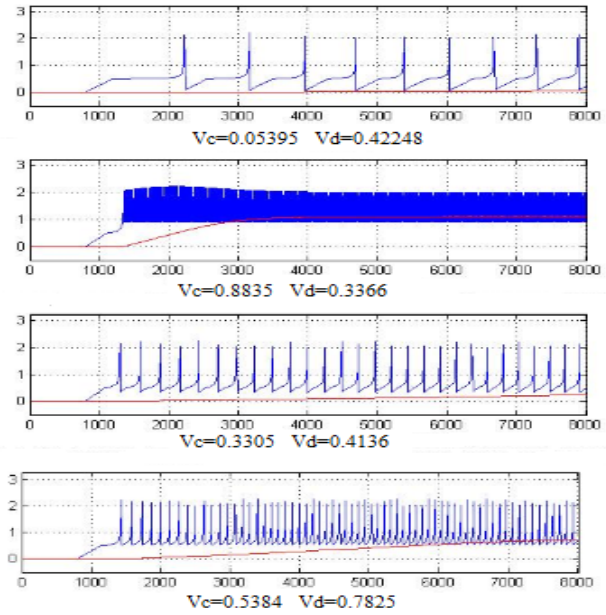

Figure 9. Spikes for different Vc and Vd parameters

Compared to other neuron circuits, this circuit has some advantages. First of all it uses only 14 transistors and using the new comparator circuit we reduced the number of transistors to 12. Contrary to otner neuron circuits, this circuit is able to produce many different neuron spikes only with changing two bias voltages Vc and Vd. You can see some of them in Figure 9.

There are five kinds of storage types for the weights: capacitor only, capacitor with refreshment, capacitor with EEPROM, digital, mixed D/A circuits. Because of the leakage problem and area constraints, capacitor weights are the least wanted solution. It is possible to solve the leakage problem using capacitor weights with refreshment but they need off chip memory. EEPROM memories are nonvolatile but they are hard to program and process sensitive. Although, digital weight usage is preferable to implement learning, higher bit resolution would be needed. However in terms of power consumption, for the neuron part analog design and for the weight part digital design is preferred[7].

4. CONCLUSION

The ADC circuit explained in this paper is a good candidate for a neuron circuit because of its low power consumption and speed. For a 0.6 um CMOS technology our ADC circuit consumes 14.2 mW average power. Also using inverter as a comparator in the neuron circuit we have seen a 17% power reduction.

5. REFERENCES

[1] E. M. Izhikevich, *Simple Model of Spiking Neurons,* IEEE Trans. Neural Networks 14 (2003) 1569-1572

[2] Jayawan H. B. Wijekon, Piotr Dudek, *Simple Analogue VLSI Circuit of a Cortical Neuron.* In IEEE int. conf. on electronics, circuits and systems (2006) 1344-1347

[3] Jayawan H. B. Wijekon, Piotr Dudek, *Spiking and Bursting Firing Patterns of a Compact VLSI Cortical Neuron Circuit* . In int. join conf. on neural network (2007) 1332-1337

[4] A. Tangel and K. Choi, *The CMOS Inverter as a comparator in ADC designs* Proc. Electrical Electronics Engineering, pp. 1-5,Nov. 2001.

[5] D. Lee, J. Yoo, K. Choi, and J. Ghaznavi, *Fat tree encoder design for ultrahigh speed flash A/D converters* in Proc. 45th Midwest Symp. Circuits and Systems, vol. 2, Aug. 2002, pp. II 87–90.

[6] S. Song, *A high speed flash analog to digital converter using a new type of quantizer. Master's thesis*, The Pennsylvania State University, 2000.

[7]V. Kakkar, *Comparative Study on Analog and Digital Neural Networks,* IJCSNS, Vol9 No7, July 2009